We claim:

1. A circuit configuration for driving a programmable link, comprising:

a volatile memory having an address input and a volatile memory cell connected to said address input for feeding in an information item, said volatile memory coupled to the programmable link for permanently storing a datum from said volatile memory cell to the programmable link; and

a shift register having a register cell coupled to said volatile memory cell in a read direction and in a write direction for a data transfer between said register cell and said volatile memory cell.

2. The circuit configuration according to claim 1, further comprising:

a write input;

a write transistor having a control input connected to said write input, and a controlled path coupled between said register cell and said volatile memory cell in the write direction;

a read input; and

a read transistor having a control input connected to said read input and a controlled path coupled between an output of said volatile memory cell and said shift register.

3. The circuit configuration according to claim 1, further comprising a drive circuit for driving the programmable link with an energy pulse, said drive circuit being coupled to said volatile memory cell for receiving a data signal.

4. The circuit configuration according to claim 3, wherein said drive circuit for controlling a provision of the energy pulse is coupled to said shift register for receiving an activation signal.

5. The circuit configuration according to claim 4, wherein said drive circuit has an AND logic circuit for combining a data input with an activation input in a logical AND combination and an output coupled to the programmable link.

6. The circuit configuration according to claim 3, wherein said drive circuit has a blowing transistor with an input side coupled to said volatile memory cell and an output connected to the programmable link, said blowing transistor providing the energy pulse in a manner dependent on the data signal and an activation signal.

7. The circuit configuration according to claim 1, wherein said shift register has a first clock signal input, a first switch on an input side connected to said first clock signal input for controling said first switch, a second clock signal input, and a second switch on an output side connected to said second clock signal input for controling said second switch.

8. The circuit configuration according to claim 7, wherein said first and second switches are CMOS transfer gates.

9. The circuit configuration according to claim 7, wherein said shift register has a further register cell with an output connected to said second switch, said second switch connected downstream of said register cell.

10. The circuit configuration according to claim 1, wherein the circuit configuration is constructed using CMOS circuit technology.

11. A memory chip, comprising:

a programmable link; and

a circuit configuration for driving said programmable link for replacing a defective memory cell with a redundant memory cell, said circuit configuration containing:

a volatile memory having an address input and a volatile memory cell connected to said address input for feeding in an information item, said volatile memory coupled to said programmable link for permanently storing a datum from said volatile memory cell to said programmable link; and

a shift register having a register cell coupled to said volatile memory cell in a read direction and in a write direction for a data transfer between said register cell and said memory cell.

12. A circuit configuration, comprising:

a programmable link;

a volatile memory having an address input and a volatile memory cell connected to said address input for feeding in an information item, said volatile memory coupled to said programmable link for permanently storing a datum in said programmable link; and

a shift register having a register cell coupled to said

volatile memory cell in a read direction and in a write

direction for a data transfer between said register cell and

said memory cell.